



# **miriac SBC-LS1088A**

**User Manual (CRX05 Revision 2+3)**

**V 2.5**

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# 1 General Notes

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## 1.5 Symbols, Conventions and Abbreviations

### 1.5.1 Symbols

Throughout this document, the following symbols will be used:



*Information marked with this symbol MUST be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment*



*Information marked with this symbol MUST be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.*



*Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features.*

Table 1-1 Symbols

### 1.5.2 Conventions

Symbol	explanation
#	denotes a low active signal
←	denotes the signal flow in the shown direction
→	denotes the signal flow in the shown direction
↔	denotes the signal flow in both directions
→	denotes the signal flow in the shown direction with additional logic / additional ICs in the signal path
I/O	denotes a bidirectional pin
Input	denotes an input pin
matched	denotes the according signal to be routed impedance controlled and length matched
Output	denotes an output pin
Pin 1	refers to the numeric pin of a component package
Pin a1	refers to the array position of a pin within a component package
XXX-	denotes the negative signal of a differential pair
XXX+	denotes the positive signal of a differential pair
XXX	denotes an optional not mounted or fitted part

Table 1-2 Conventions

## 2 Introduction

Thank you for choosing the MicroSys SBC-LS1088A Single Board Computer system. This manual should help you to get the best performance and details out all of its features.

### 2.1 Safety and Handling Precautions



DANGER

**ALWAYS use the correct type and polarity of the power supply!**

**DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.**

**ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.**



ATTENTION

**Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns, and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.**



ATTENTION

**ALWAYS take care of ESD-safe handling!**

**Many pins on external connectors are directly connected to the CPU or other ESD sensitive devices.**

**Make or break ANY connections ONLY while the unit is switched OFF.**

**Otherwise, permanent damage to the unit may occur, which is not covered by warranty.**



NOTE

**There is no separate SHIELD connection.**

**All the metal sheaths of shielded connectors are connected to GND.**

**Also, all mounting holes of the carrier board are connected to GND.**

**The module's mounting holes are not connected to GND**

**Take this into account when handling and mounting the unit.**

Table 2-1 Safety and Handling Precautions

## 2.2 Short Description

The SBC-LS1088A is a small computer system consisting of

- the MPX-LS1088A module, based on NXP's LS1088A Multicore Communications Processors
- and the CRX05 carrier board.

It targets both

- evaluation of the respective MPX-LS1088A SOM
- direct usage as an industrial computing solution

This document gives you an overview on the board's connectors and how to take the first steps on the initial setup.

## 2.3 Shipping List

The SBC-LS1088A EvalKit package contains the following items:

- The SBC-LS1088A system, mounted with cooling solution
- Power Supply 12V DC stabilized / 2 A
- Cable adapter for the power supply
- USB cable type A – mini B
- Micro-SD-Card with U-Boot and root file system

## 2.4 Feature Changelog for HW Revisions

### 2.4.1 Changes from revision 2 to revision 3

The revision 3 of the carrier board provides the following changes:

- Added SW4 to switch between root complex and endpoint
- Added 2 header for GND interconnection (JP1, JP2)
- Added buffer to SPI-CLK
- Added possibility to modify board to run with external PCIe-clock, requires hardware modification (default assembled to use internal clock)
- Type of "JTG-connector" changed to JST-BM14B-SRSS-TB

## 2.4.2 Changes from revision 1 to revision 2

The revision 2 of the carrier board provides new features:

- Added LED driver with 4x RGB LEDs
- Added 12 GPIOs (6x in / 6x out) addressable via I<sup>2</sup>C
  - Output voltage level maximum 24V (according to the input voltage of the carrier board)
  - Input voltage range 24V maximum
- Added SuperCap for RTC backup battery (CR2032 coin cell as assembly option still available)
- Added prerequisites for support of emBRICK devices
- Added current shunt for current measurements
- Added optional (by assembly option) support for onboard current measurements of the CPU module consumption via I<sup>2</sup>C current sense amplifier
- Added LAN interrupt support
- Added SMART CARD connector
- Added optional (by assembly option) extension connector (for example for additional GPIOs or graphic support if provided by the CPU)
- Added mounting holes for the carrierboard
- Added a fan connector
- Added connector labeling (silkscreen) on the PCB

Some features were changed:

- SerDes 6 and SerDes 7 lanes were swapped in order to achieve a wider functional coverage within the MPX2 module family
  - SerDes 6 is now connected to the SATA connector (ST10)
  - SerDes 7 is now connected to the mPCIe / mSATA slot (ST7)
- Improved power input section with filters
- Improved mechanical mounting of the CPU module and mPCIe/ mSATA cards
- Replaced PCIe x1 edge card connector with second PCIe extension connector

## 2.5 Functional Coverage

The following table shows the coverage achieved by the SBC-LS1088A compared to the features which are available on the carrierboard:

Interfaces provided by CRX05 carrierboard		Interfaces available with the SBC-LS1088A
SerDes 0	PCIe	✓
SerDes 1	SGMII	✓
SerDes 2	SGMII	✓
SerDes 3	SGMII	✓
SerDes 4	mPCIe / Aurora	✓ (mPCIe)
SerDes 5	PCIe	✓
SerDes 6	SATA	-
SerDes 7	mPCIe / mSATA	✓
RGMII 1	PHY	✓
USB 1	2.0 / 3.0	✓ (3.0)
USB 2	2.0 / 3.0	✓ (3.0)
SD-Card	1bit / 4 bit & boot device	✓
UART 1	UART to USB (debug console)	✓
UART 2	TTL only	✓
I <sup>2</sup> C 1	Multiple devices	✓
I <sup>2</sup> C 2	Multiple devices	-
JTAG	Signals on non-standard connector	✓
Watchdog	Hardware watchdog with trigger signal from module	✓
RTC backup	Supercap	✓
Manual Reset	Button	✓
Reset LEDs	2x red	✓
Power LED	1x green	✓

Table 2-2 Functional coverage

## 3 Quick Start Guide

### 3.1 Prerequisites



*Always make sure to handle the SBC-LS1088A unit ESD-safe!*

*Otherwise, the unit may suffer permanent damage.*

*However, do not place the unit directly flat on a metal surface,  
as this may result in short circuits and damage to the board.*

At first time operation unpack the unit and make sure that is clean and free of visible damage or foreign objects.

#### 3.1.1 Minimum Requirements

To operate the board, you will at least need the following items:

- an adequate power supply, delivering 12V DC (stabilized) / 2A minimum.
- an USB cable (type A – mini B) adapted to connector ST5
- a serial terminal, such as a PC with an USB port running a terminal Software (e.g. TeraTerm, HyperTerminal, putty, ckermit...), or else a hardware serial console. **Choose the following parameters:**

- (a) **115200 Bd**
- (b) **8 Data bits**
- (c) **No parity**
- (d) **1 Stop Bit**

#### 3.1.2 Recommended Items

The following items are not absolutely necessary, but strongly recommended for practical operation and development purposes:

- Network connection via Port1 to your local network installation
- TFTP server available for downloading within the network (Hint: may run on the same PC as the serial Terminal)
- SATA HDD/SSD and/or SD card as mass storage and/or boot media

## 3.2 Board Preparation and Power-Up

- Make sure the switches SW1 and SW2 are set properly in order to select the correct boot source and board configuration
- The board comes preconfigured to boot correctly on arrival.
- Connect the mini USB cable to ST5.
- Connect other peripherals (USB, LAN, SATA, ...) as far as intended.
- Connect the power line to the ST3 connector, while the power supply is still switched off.
- Switch on the power.

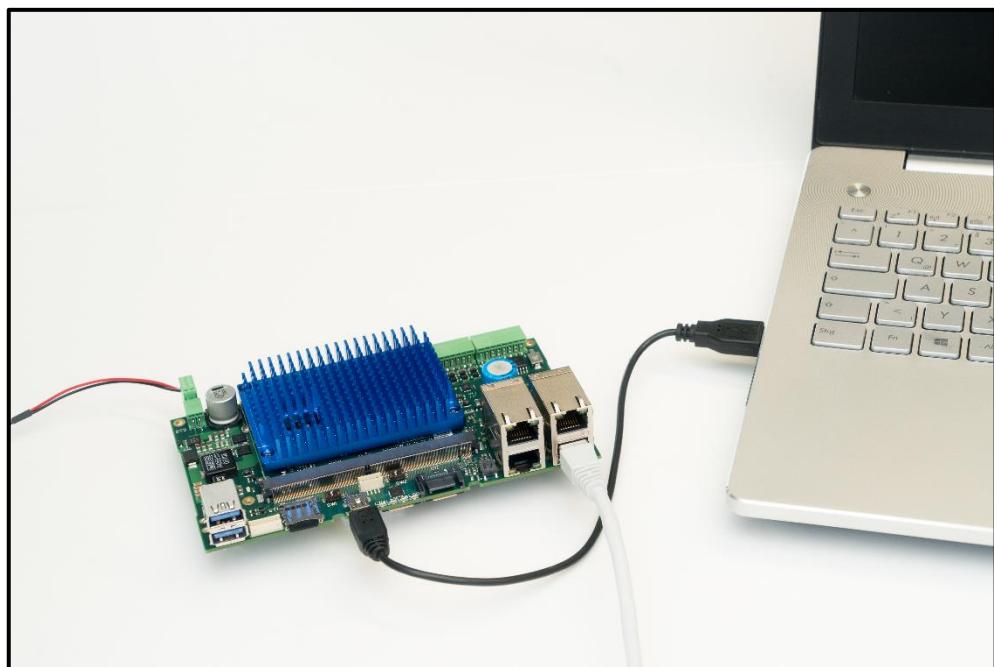


Figure 3-1 System setup example (LAN port 1)

## 3.3 Operation



**After Power-up, the green LED on the module should light up and any red LED should be off.**

**IF NOT, DISCONNECT THE UNIT FROM POWER AND CHECK FOR FAULTS!**

### 3.3.1 U-Boot Startup

When power is supplied the system will start.

On startup, U-Boot will come up similar to the following:



**The exact output may vary, depending on U-Boot and MPX-LS1088A module versions in use.**

```
U-Boot SPL 2016.012.0+g624c887 (Feb 08 2017 - 14:42:03)
Initializing DDR....using SPD
Address hashing enabled.
Trying to boot from MMC
```

```
U-Boot 2016.012.0+g624c887 (Feb 08 2017 - 14:42:03 +0100)
```

```
SoC: LS1088E Version:1.0 (0x87030010)
Clock Configuration:
    CPU0(A53):1400 MHz   CPU1(A53):1400 MHz   CPU2(A53):1400
MHz
    CPU3(A53):1400 MHz   CPU4(A53):1400 MHz   CPU5(A53):1400
MHz
    CPU6(A53):1400 MHz   CPU7(A53):1400 MHz
Bus:       600 MHz   DDR:        1600 MT/s
Reset Configuration Word (RCW):
    00000000: 38004018 00000040 00000000 00000000
    00000010: 00000000 000a0000 00300000 00000000
    00000020: 00e01140 00002580 00000000 00000040
    00000030: 01800052 00000000 00000a83 00000000
    00000040: 00000000 00000000 00000000 00000000
    00000050: 00000000 00000000 00000000 00000000
    00000060: 00000000 00000000 00000000 000009e7
    00000070: 33330000 00009555 00000000 00000000
I2C: ready
Model: MicroSys Layerscape MPXLS1088 Board
Board: MPXLS1088, booting from SD card
DRAM: Detected UDIMM Fixed DDR on board
3 GiB
```

```
DDR      3 GiB (DDR4, 64-bit, CL=11, ECC on)
Waking secondary cores to start from ffff1c000
All (8) cores are up.
Using SERDES1 Protocol: 18 (0x12)
Using SERDES2 Protocol: 13 (0xd)
NAND: 512 MiB
MMC: FSL_SDHC: 0
PCIe1: Root Complex no link, regs @ 0x3400000
PCIe2: Root Complex no link, regs @ 0x3500000
PCIe3: Root Complex no link, regs @ 0x3600000
In:    serial
Out:   serial
Err:   serial
SEC0: RNG instantiated
SATA link 0 timeout.
AHCI 0001.0301 32 slots 1 ports 6 Gbps 0x1 impl SATA mode
flags: 64bit ncq pm clo only pmp fbss pio slum part ccc apst
Found 0 device(s).
SCSI: Net: Device: FSL_SDHC
Manufacturer ID: 74
OEM: 4a60
Name: USD
Tran Speed: 50000000
Rd Block Len: 512
SD version 3.0
High Capacity: No
Capacity: 1.9 GiB
Bus Width: 4-bit
Erase Group Size: 512 Bytes

MMC read: dev # 0, block # 6144, count 2048 ... 2048 blocks
read: OK

MMC read: dev # 0, block # 16384, count 2048 ... 2048 blocks
read: OK
crc32+
fsl-mc: Booting Management Complex ... SUCCESS
fsl-mc: Management Complex booted (version: 10.0.2, boot status: 0x1)
DPMAC2@sgmii [PRIME], DPMAC3@sgmii, DPMAC4@rgmii,
DPMAC7@sgmii
=>
```

### 3.3.2 Linux

For detailed setup instructions, refer to the readme document delivered along with the unit!

# 4 System Description

This section describes all parts of the SBC-LS1088A system.

## 4.1 Block Diagram

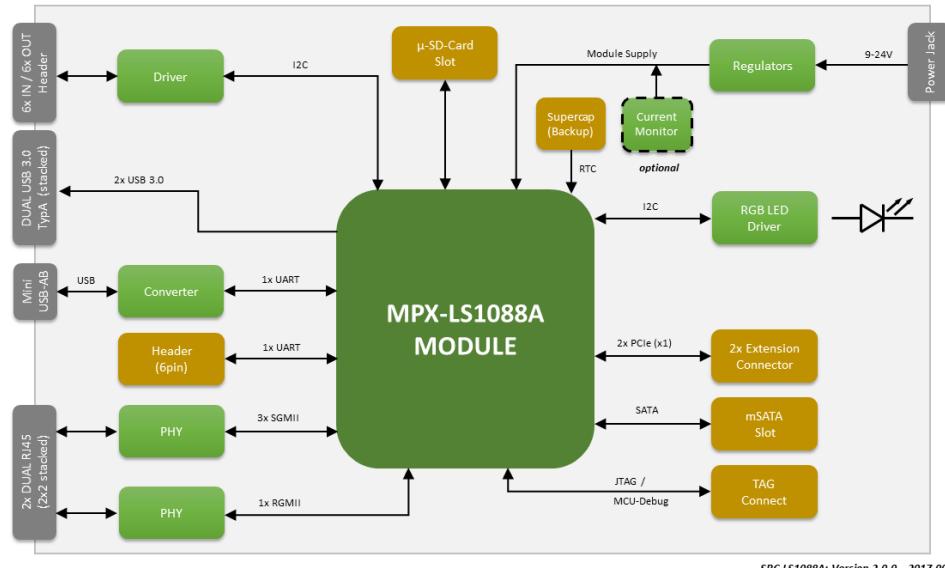


Figure 4-1 Block Diagram (MPX-LS1088A Revision 2 on carrier CRX05 Revision 2)

## 4.2 Feature Overview

The SBC-LS1088A offers the following features:

QorIQ ARM Cortex A53 cores 8xCPU Processor		
<b>SDRAM</b>	64-bit DDR4 interface	Default: 2GByte up to 4GByte up to 2100MT/s 4 x DDR4 (x16) single bank
<b>Synchronous Memory</b>	8-bit NAND Flash	Default: 512 MB up to 2 GByte
<b>Hard Disk Drives Interface</b>	SATA 3.0	mSATA slot
<b>PCI Express port</b>	3.0 / 8Gbps Lane x1 Root complex operations	2x PCIe extension connector
	3.0 / 8Gbps Lane x1 Root complex operations	1x Mini PCIe/mSata Slot
	3.0 / 8Gbps Lane x1 Root complex operations	1x Mini PCIe Slot
<b>USB</b>	USB 3.0 Phy	USB connector type A

QorIQ ARM Cortex A53 cores 8xCPU Processor		
	USB 3.0 Phy	USB connector type A
<b>Expansion Cards</b>	MMC/SD/SDIO	micro SD card holder
<b>Serial Interfaces</b>	UART1	Converted to USB (FT232), Available on USB connector type mini B
	UART2	4-wire Extension Port LVTTL
<b>I2C</b>	I2C-1	400 kbps <b>Connected Devices:</b> TMP451AIDQF Temperature Sensor 2x BR24G128NUX-3 EEPROM RX-8803 RTC IDT6V49205B Clock Generator TLC59116 RGB LED Driver MAX7325 GPIO Port Expander
	I2C-4	400 kbps
<b>Gigabit Ethernet Controller</b>	RGMII	10/100/1000 Mbps
	SGMII	10/100/1000 Mbps
	SGMII	10/100/1000 Mbps
	SGMII	10/100/1000 Mbps
<b>System JTAG Controller</b>	JTAG	Different connector on CRX05-R2 and R3
<b>Power Management</b>	Primary Supply	LM25116MH <b>Input:</b> 9-24V DC <b>Output:</b> 5V DC / peak 8A
	Backup Supply (RTC backup)	Supercap

Table 4-1 Feature Overview

## 4.3 Mechanical Dimensions

### 4.3.1 MPX-LS1088A

The following drawing shows the mechanical outline of the MPX-LS1088A module that is plugged in the CRX05 carrier board.



This drawing is not to scale.



For 3D data files please contact MicroSys.

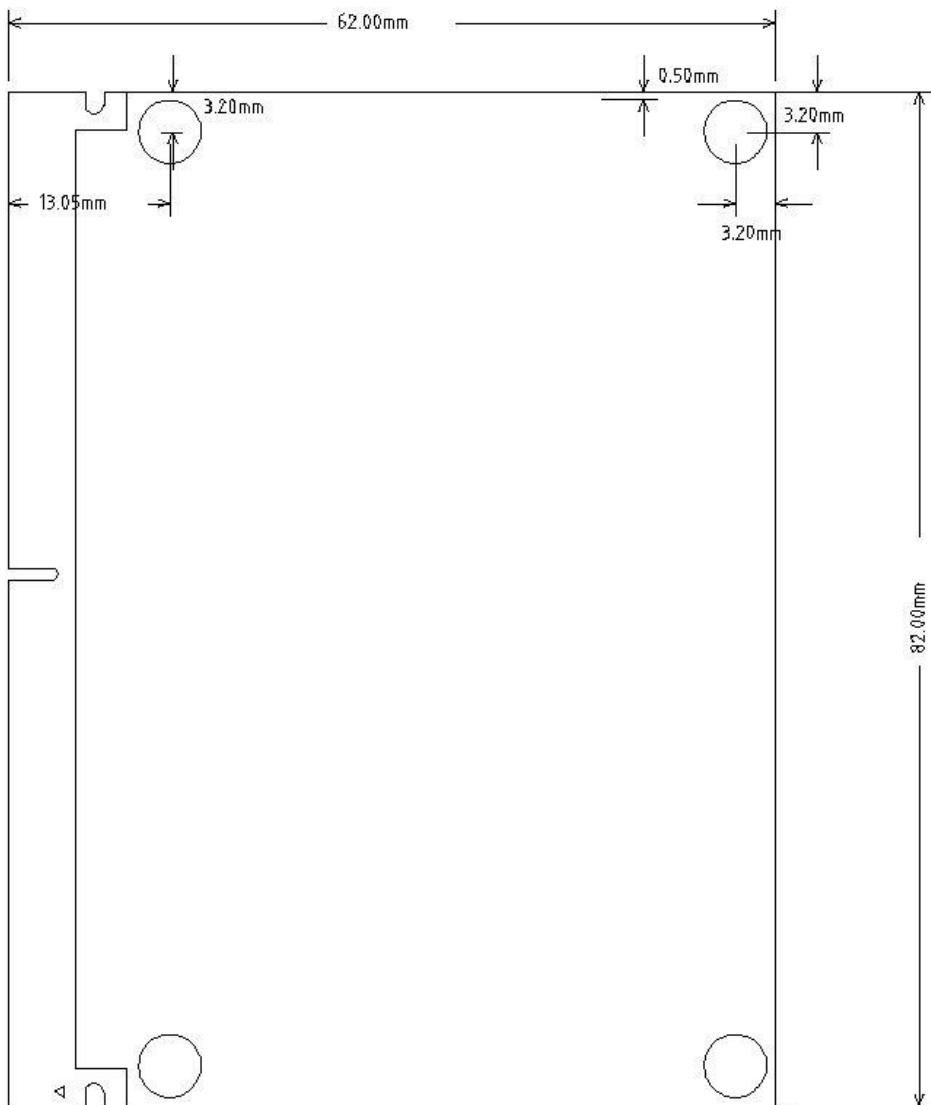


Figure 4-2 Mechanical Dimensions Modul

#### 4.3.2 SBC-LS1088A

The following drawing shows the mechanical outline of the SBC-LS1088A assembly.



This drawing is not to scale.



For 3D data files please contact MicroSys.

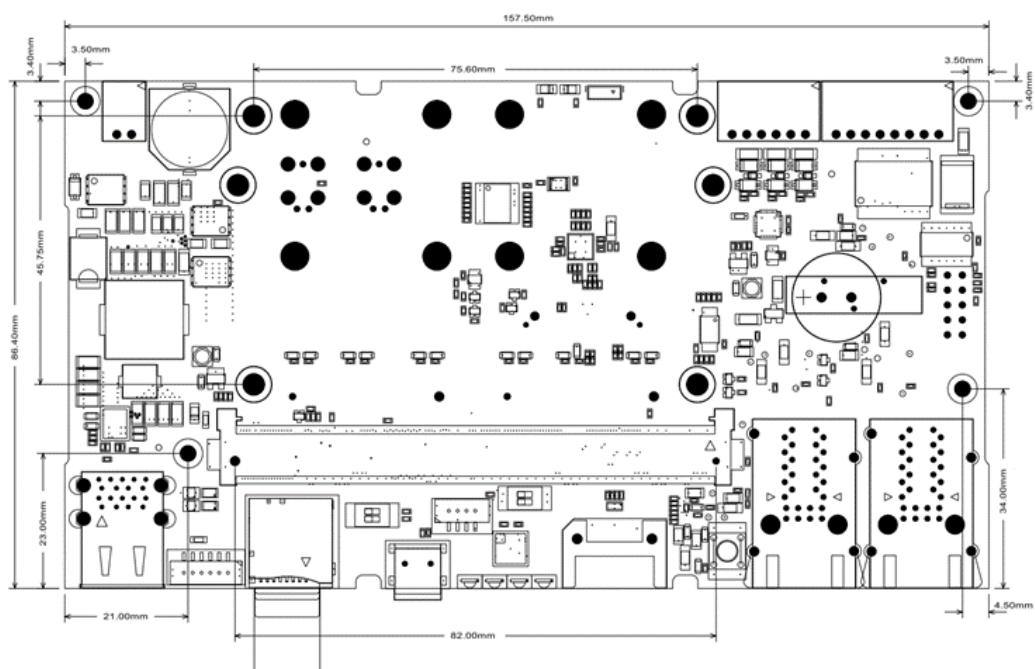


Figure 4-3 SBC-LS1088A Mechanical Dimensions

## 4.4 Connector Layout – Top

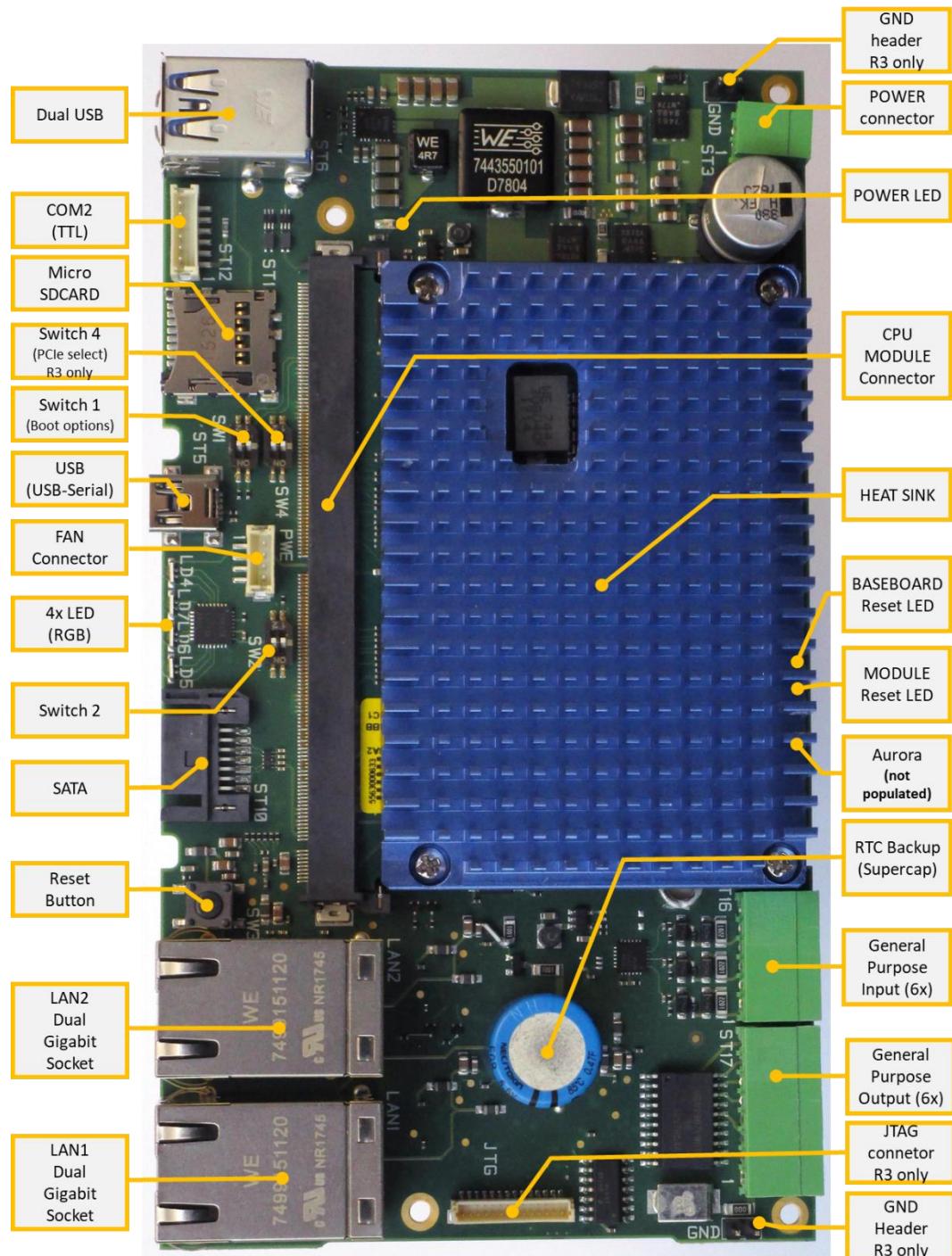


Figure 4-4 Top connectors

## 4.5 Connector Layout – Bottom

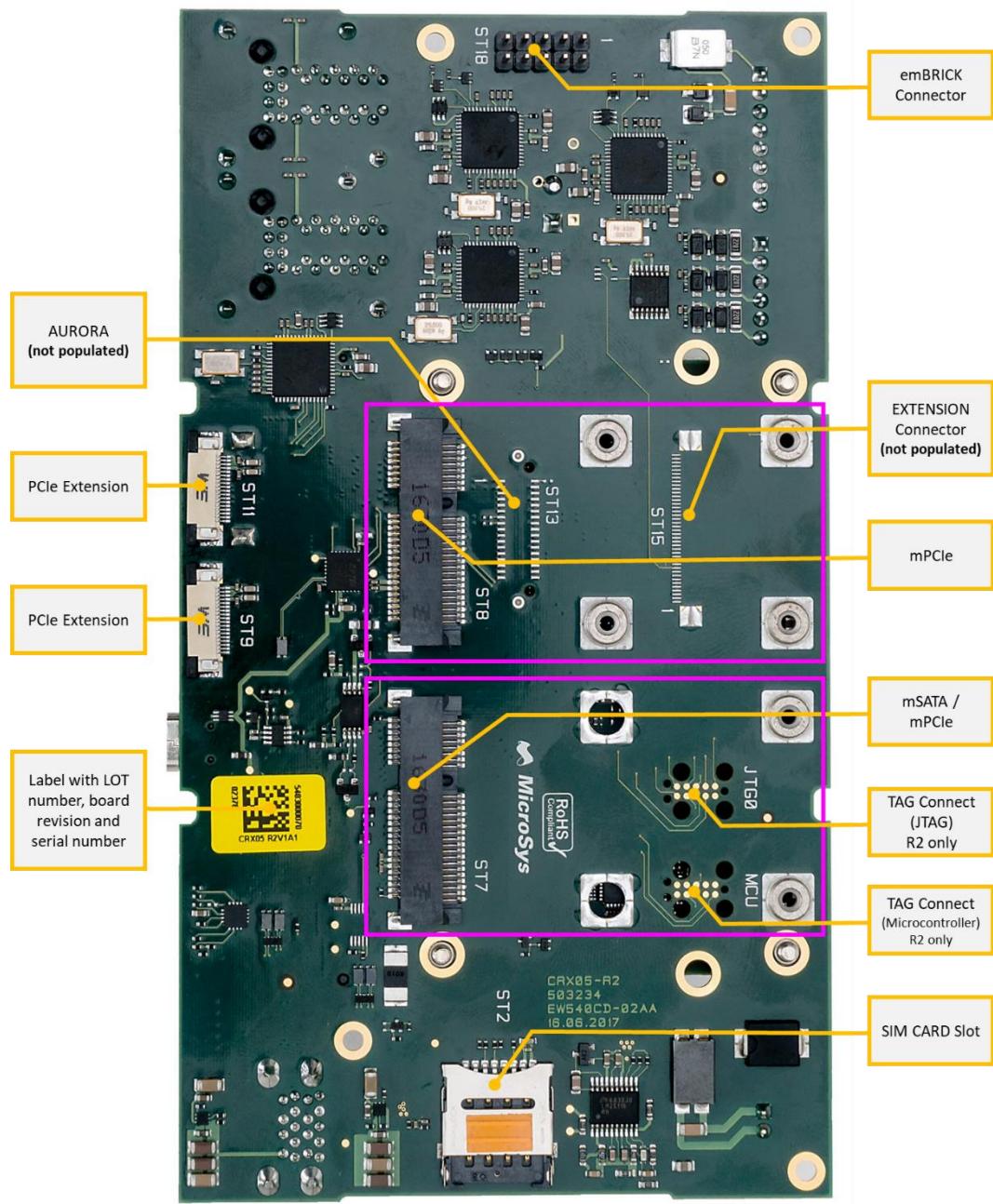


Figure 4-5 Bottom connectors

## 4.6 Power Supply

### 4.6.1 Input Supply Rating

The SBC-LS1088A system is run from a single DC power supply with the following ratings:

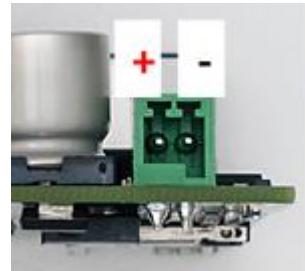
<b>Maximum Input Voltage Operating Range:</b>	<b>9V - 30V DC</b>
<b>Nominal Input Supply Voltage:</b>	<b>12V DC</b>
<b>Typical Current Consumption (@12V / room temperature / U-boot prompt):</b>	<b>-0,77A</b>



**ALWAYS use the correct type and polarity of the power supply!**  
**DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.**

### 4.6.2 Input Power Connector

Part Reference	ST3
Manufacturer:	Würth Elektronik
Type:	691 382 010 002
Mates with:	691 381 000 002 (included in delivery)



Pin-out:

Pin	Name	Function
1	,，“+	+VIN (= typ. 12V)
2	,，“-	GND

Table 4-1 Pinout ST3

### 4.6.3 Power Supply Structure

- Input Power from ST3 connector is fed to the primary step-down converter.
- The primary step-down converter produces 5V DC / max. 8A peak from the input supply which supplies both the LS1088A module and peripheral devices on the carrierboard CRX05.

- The 5V DC are fed to a secondary step-down converter, which produces 3.3V DC / max. 4A peak.
- Two NCP1529 produce 1.8V and 1.5V from 3.3V, which are used for both PCIe and onboard devices.

The following diagram shows the Power Supply structure:

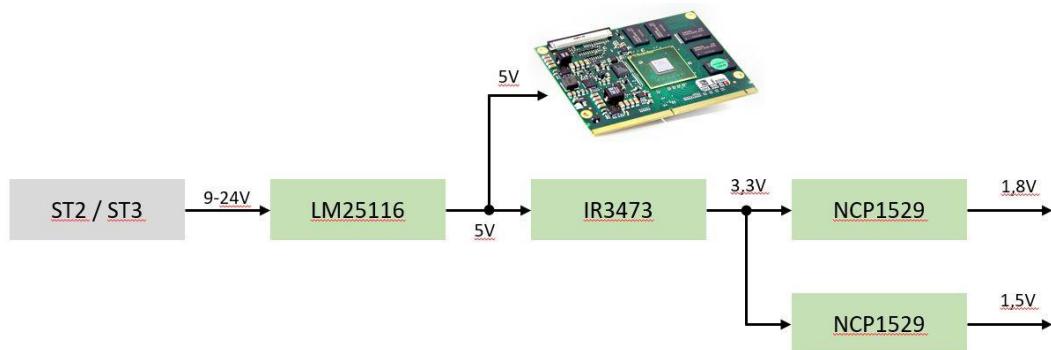


Figure 4-6 Power supply structure

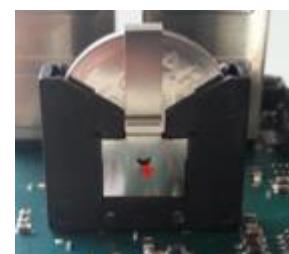
#### 4.6.4 RTC Backup Battery

The RTC on the module is supplied from a 470mF supercap that is loaded by the 5V power source on the carrier board.



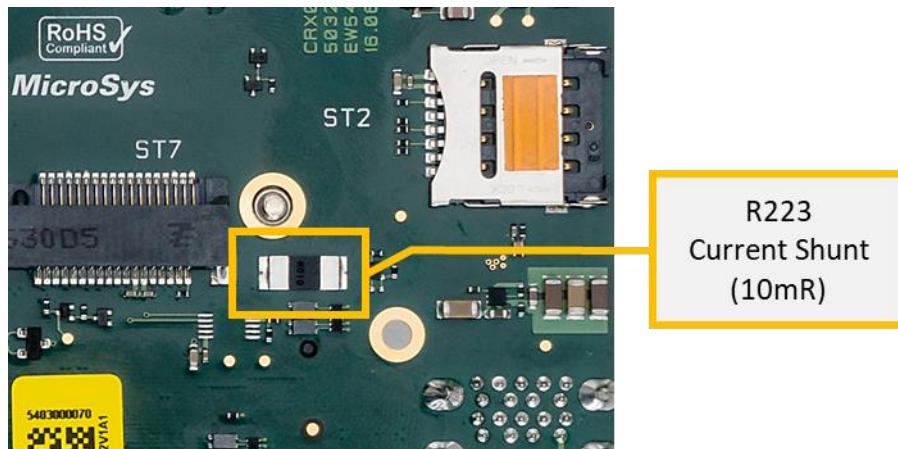
Alternatively, there's another version of the carrier board available that has a backup battery holder for CR2032 batteries. Please contact MicroSys for more information.

Part Reference:	BAT1
Manufacturer:	Renata Batteries
Type:	VBH2032-1
Used with:	CR2032 batteries



#### 4.6.5 Current Measurement

For current measurements the carrierboard provides a 10mΩ shunt resistor in the 5V path supplying the CPU module.



For automated measurements there's a carrierboard version available that already provides an I<sup>2</sup>C current sense amplifier.



*The current sense amplifier is not populated by default.*

*For more information please contact MicroSys.*

#### 4.6.6 Fuses

There are no fuses on the SBC-LS1088A.

# 5 System Core, Boot Configuration and On-Board Memory

## 5.1 Processor NXP LS1088A

The LS1088A Processor by NXP is a QorIQ Layerscape CPU with four CPU cores. It exposes a wide variety of external interfaces, which are explained in detail in the following chapters. The cores share a single 2MB L2 Cache.

The four CPU cores run at a maximum clock speed of 1600 MHz, 1400 MHz or 1000 MHz respectively, depending on the ordered type. The CPU frequency can be clocked down if necessary.

## 5.2 JTAG Chain

The JTAG chain of the SBC-LS1088A includes the LS1088A processor only. The JTAG port is directly connected to the connector “JTG0”.

The JTAG connector footprint provides JTAG signals. For interfacing standard debugger pinouts an additional intermediate adapter is necessary.

Please see chapter 6.10 for a description of the JTAG connector.

## 5.3 Reset Structure

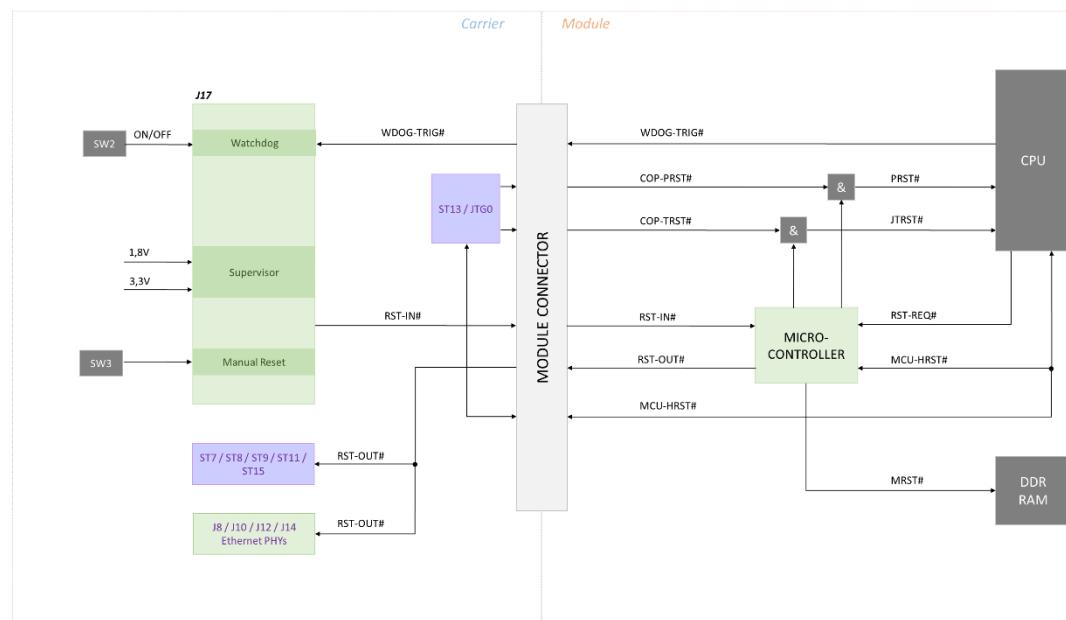


Figure 5-1 Reset Structure (carrier CRX05 Revision 2)

Pin Number on ST4	Signal Name	Signal Direction	Function
T136	RST-IN#	Input to the module	Active low module reset: while active the module is held in reset state
T135	RST-OUT#	Output from the module	Active low peripheral reset: while active peripheral devices shall be held in reset state
B118	WDOG-TRIG#	Output from the module	Watchdog service signal from the module which has to be triggered periodically. When the watchdog is active and the service stops the module will be reset.
B111	MCU-HRST#	Bi-directional	Please contact MicroSys
B110	COP-PRST#	Input to the module	Please contact MicroSys
B106	COP-TRST#	Input to the module	Please contact MicroSys

Table 5-1 Reset signal overview



**The default state for RST-IN# is active. Consequently, the module is always in a reset state when the RST-IN# signal is not actively driven high by the carrierboard.**

The RST-IN# is an input to the module. It signals that the voltage supplies on the carrierboard are within their limits and no manual reset is triggered. When active (signal is low) the microcontroller unit on the module initiates the reset sequence in order to keep the CPU in a defined reset state. No further interaction from the carrierboard is necessary. In case the module reset is active, the module triggers the RST-OUT# signal which is intended to control the reset of peripheral devices on the carrierboard i.e. Ethernet PHYs, PCIe slots and devices.

The RST-IN# signal can be triggered by either a power fault situation, a manual reset button press (SW3) or a missing watchdog trigger signal WDOG-TRIG# from the CPU in case the watchdog has been manually enabled beforehand via SW2.

MCU-HRST#, COP-PRST# and COP-TRST# are for JTAG and debugging purposes only.



**The watchdog is off by default.**

**The watchdog is implemented on the carrier board.**

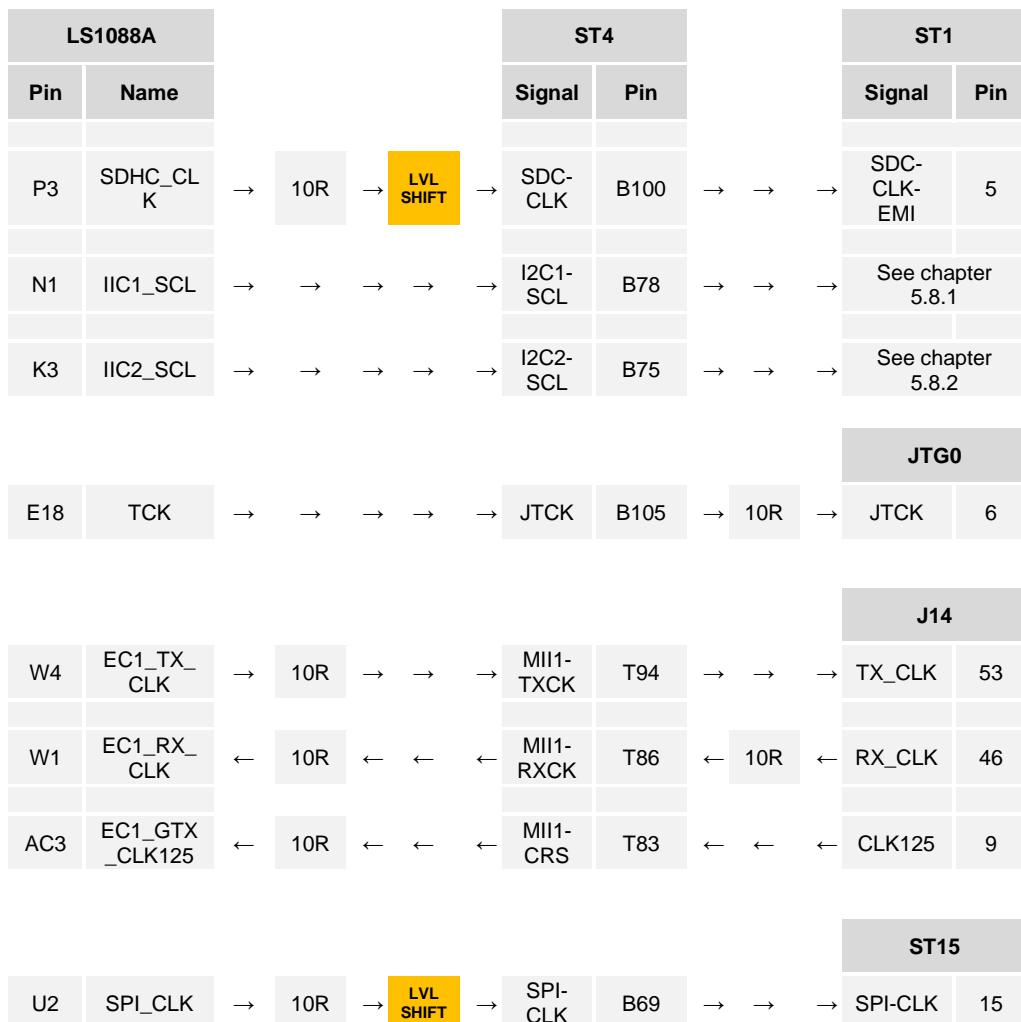
The following voltages on the carrier board are monitored by a Maxim MAX6751KA29 chip:

Voltage	Monitoring	Voltage Limit
3,3V	Undervoltage	Typ. 2,925V [2,867V-2,984V]
1,8V	Undervoltage	Typ. 1,72V [1,69V-1,75V]

Table 5-2 Voltage monitoring limits (carrier)

## 5.4 Clock Distribution

The following diagram shows the clock distribution of the SBC-LS1088A system



IDT6V49205B		LS1088A	
Pin	Name	Name	Pin
23	PCIeT_LR0	SD1-REFCLK1	AA8
24	PCIeC_LR0	SD1-REFCLK1 #	AB8
26	PCIeT_LR1	SD1-REFCLK2	AB18
25	PCIeC_LR1	SD1-REFCLK2 #	AB19

		ST4		J6	
		Signal	Pin	Signal	Pin
36	PCIeT_LR4	SRD-CLK1+	T50	→	SRC 19
35	PCIeC_LR4	SRD-CLK1-	T51	→	SRC# 20

ST7			
OUT0	2	→	PCIE-CLKD+ 13
OUT0#	3	→	PCIE-CLKD- 11
ST8			
OUT1	5	→	PCIE-CLKB+ 13
OUT1#	6	→	PCIE-CLKB- 11
ST11			
OUT2	12	→	PCIE-CLKC+ A13
OUT2#	11	→	PCIE-CLKC- A14
ST9			
OUT3	15	→	PCIE-CLKA+ 7
OUT3#	14	→	PCIE-CLKA- 6

Table 5-3 Clock distribution

## 5.5 Boot Configuration

The SBC-LS1088A board offers three possible boot devices to choose from. The settings can be done via SW1 (see chapter 7 for details).

SW1 configures two signals “BOOT-SEL1” and “BOOT-SEL2” which have a default high state (10k pullups are on the module) when no connection is made or SW1 is off. When the switch is on, the respective pin is grounded.

The BOOT-SELx pins are decoded to the following configuration (1= high, 0=low):

LS1088A		BOOT-SEL2   BOOT-SEL1 =		
Signal	Pin	SDHC =[10]	SPI =[11]	NAND =[01]
IFC_AD08	A12	0	1	t.b.d
IFC_AD09	A13	0	0	t.b.d
IFC_AD10	B14	0	0	t.b.d
IFC_AD11	A14	0	0	t.b.d
IFC_AD12	B15	0	1	t.b.d
IFC_AD13	A15	1	1	t.b.d
IFC_AD14	A16	0	0	t.b.d
IFC_AD15	A17	0	0	t.b.d
IFC_CLE	C19	0	0	t.b.d

Table 5-4 Hard wired boot signals

## 5.6 NAND Flash

The SBC-LS1088A system is equipped with 2GB of NAND Flash by default. Different sizes may be available on request/order. The following table shows the connections and signal levels for the NAND Flash.

I/O Range	NAND Flash		SBC-LS1088A		LS1088A		Description	
	Pin	Name	Signal		Pin	Name		
1,8V	G5	<i>LOCK</i>					Lock	
1,8V	C8	<i>RY/BY</i>	→	IFC-RB0#	→	C16	<i>IFC_RB0#</i>	ready/busy, 4,7K pullup
1,8V	D4	<i>RE#</i>	←	IFC-OE#	←	C18	<i>IFC_OE#</i>	read enable
1,8V	C6	<i>CE#</i>	←	IFC-CS0#	←	C17	<i>IFC_CS0#</i>	chip select
1,8V	D3,G4,H8, J6	VCC		+1.8V				
	C5,F7,K3, K8	GND		GND				
1,8V	D5	<i>CLE</i>	←	IFC-CLE	←	C19	<i>IFC_CLE</i>	command latch enable
1,8V	C4	<i>ALE</i>	←	IFC-AVD	←	A18	<i>IFC_AVD</i>	address latch enable
1,8V	C7	<i>WE#</i>	←	IFC-WE#	←	C15	<i>IFC_WE0#</i>	write enable
1,8V	C3	<i>WP#</i>	←	IFC-WP#	←	D19	<i>IFC_WP0#</i>	write protect
1,8V	H4	<i>D0</i>	↔	IFC-AD7	↔	B12	<i>IFC_AD0</i>	data line
1,8V	J4	<i>D1</i>	↔	IFC-AD6	↔	A11	<i>IFC_AD1</i>	data line
1,8V	K4	<i>D2</i>	↔	IFC-AD5	↔	B11	<i>IFC_AD2</i>	data line
1,8V	K5	<i>D3</i>	↔	IFC-AD4	↔	A10	<i>IFC_AD3</i>	data line
1,8V	K6	<i>D4</i>	↔	IFC-AD3	↔	A9	<i>IFC_AD4</i>	data line
1,8V	J7	<i>D5</i>	↔	IFC-AD2	↔	B9	<i>IFC_AD5</i>	data line
1,8V	K7	<i>D6</i>	↔	IFC-AD1	↔	A8	<i>IFC_AD6</i>	data line
1,8V	J8	<i>D7</i>	↔	IFC-AD0	↔	B8	<i>IFC_AD7</i>	data line
	G3	<i>n.c.</i>						Not connect
	G8	<i>n.c.</i>						Not connect

Table 5-5 NAND Flash pin assignments

## 5.7 QSPI Flash

The SBC-LS1088A system is equipped with 16MB of QSPI Flash on the LS1088A's QSPI port. Up to 64 MB are available on request/order.

The following table shows the internal connections:

I/O Range	QSPI Flash MT25QU128ABA8E12		LS1088A	
	Pin	Name	Pin	Name
LVttl	C2	CS	← D8	QSPI_A_CS0
LVttl	B2	CLK	← C9	QSPI_A_SCK
	B3	GND	←	
LVttl	D3	D0	↔ D11	QSPI_A_DATA0
LVttl	D2	D1	↔ C12	QSPI_A_DATA1
LVttl	C4	D2	↔ D13	QSPI_A_DATA2
LVttl	D4	D3	↔ C13	QSPI_A_DATA3
	B4	+1.8V		

Table 5-6 QSPI Flash pin assignment

## 5.8 I<sup>2</sup>C Bus

The SBC-LS1088A offers two independent I<sup>2</sup>C busses.

The following tables show the I<sup>2</sup>C addresses as 7 Bit addresses. The R/W bit is not displayed.

### 5.8.1 I<sup>2</sup>C-1

I<sup>2</sup>C Bus 1 (7-Bit address):

Address	Device	Function
0x32	RX-8803LC	RTC
0x00	TMP451AIDQF	General Call reset address
0x4C		Temperature sensor
0x50	BR24G128NUX-3	EEPROM (on module)
0x57 / (0x55) Selectable via SW2 (see 7.2)	BR24G128NUX-3	EEPROM (on carrier)
0x58	MAX7325ATG	Port Expander GP output address
0x68		Port Expander GP input address
0x60	TLC59116IRHBR	RGB LED Driver Slave Address
0x68		All Call Address <b>(must be disabled!)</b>
0x6B		Software Reset Address
0x69	IDT6V49205BNLGI	Clock Generator

Table 5-7 I<sup>2</sup>C1 bus map



**I<sup>2</sup>C address 0x68 is existing twice on I<sup>2</sup>C-1 bus.**

**Therefore, the so-called “All Call I<sup>2</sup>C address” of the TLC59116IRHBR RGB LED driver has to be disabled before GP input pins of the MAX7325 port expander can be read correctly. This can be achieved by setting the default value 1 of Bit 0 in MODE1 register to 0.**

The I<sup>2</sup>C Bus 1 has the following layout:

I/O Range: LVTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
LS1088A	IIC1_SCL	N1	IIC1_SDA	M1
	↓		↑	
RX-8803LC	SCL	5	SDA	8
	↓		↑	
BR24G128NUX-3	SCL	6	SDA	5
	↓		↑	
TMP451AIDQF	SCK	8	SDA	7
	↓		↑	
IDT6V49205B	SCLK	46	SDATA	47
	↓		↑	
Module Connector	I2C1_SCL	B78	I2C1_SDA	B77
	↓		↑	
MAX7325	SCL	19	SDA	20
	↓		↑	
BR24G128NUX-3	SCL	6	SDA	5
	↓		↑	
TLC59116IRHBR	SCL	25	SDA	26

Table 5-8 I<sup>2</sup>C-1 pin assignment

### 5.8.2 I<sup>2</sup>C-2 (not available)



ATTENTION

**I<sup>2</sup>C-2 is not available with the LS1088A**

### 5.8.3 I<sup>2</sup>C-4



ATTENTION

**I<sup>2</sup>C-4 is available without hardware modifications.**

**Unlike SBC-LS1046A and SBC-LS1043A I<sup>2</sup>C-4 can be accessed on pins B7 (SDA) and B13 (SCL)**

No devices or connectors are connected to I<sup>2</sup>C-4 port on the CRX05.

# 6 Peripherals

## 6.1 Connector References

Reference	Function	Populated?	Top / Bottom
ST1	Micro SD slot	✓	Top
ST2	Smart Card connector	✓?	Bottom
ST3	Power connector	✓	Top
ST4	CPU Module Connector	✓	Top
ST5	USB to serial connector	✓	Top
ST6	Dual USB connector	✓	Top
ST7	mPCIe / mSATA slot	✓	Bottom
ST8	mPCIe slot	✓	Bottom
ST9	PCIe extension connector	✓	Bottom
ST10	SATA connector	✓	Top
ST11	PCIe extension connector	✓	Bottom
ST12	UART2 connector	✓	Top
ST13	Aurora connector 1	-	Bottom
ST14	Aurora connector 2	-	Bottom
ST15	Extension connector	-	Bottom
ST16	GPIR connector	✓	Top
ST17	GPOUT connector	✓	Top
ST18	emBRICK connector	✓	Bottom
PWE	Fan connector	✓	Top
LAN1	RJ45 connector	✓	Top
LAN2	RJ45 connector	✓	Top
MCU	Microcontroller	TAG connect	Bottom R2 only
JTG0	JTAG connector	TAG connect JST-BM14-SRSS	Bottom (R2) Top (R3)

Table 6-1 Connector reference overview

## 6.2 Module Connector

The carrierboard CRX05 provides a connector "ST4" which accepts compatible CPU modules from the MicroSys MPX2-family.



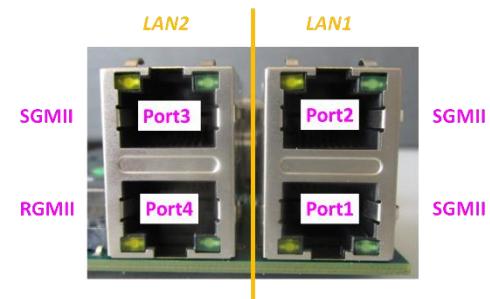
Manufacturer:	JAE
Type:	MM70-314-310-B1-1-R300
Used with:	MicroSys MPX2 module family

## 6.3 LAN Connections

The SBC-LS1088A system offers four independent Gigabit LAN connections. These three ports are distributed over two connectors named "LAN1" and "LAN2". The connectors have integrated magnetics.

The following picture shows the front view of the two connectors as placed on the CRX05 baseboard. For further information on the LEDs please see chapter 8

Part Reference:	LAN1, LAN2
Manufacturer:	Würth Elektronik
Type:	749 915 1120
Mates with:	RJ45 patch cable, category depending on speed



Port	LS1088A connection	Serdes Lane on ST4	RGMII on ST4	PHY address
1	„DPMAC2“	Lane1	---	0000
2	„DPMAC3“	Lane2	---	0001
3	„DPMAC7“	Lane3	---	0010
4	„DPMAC4“	---	RGMII1	0011

Table 6-2 LAN / DTSEC / SerDes / RGMII assignment

The LAN Sockets have a standard layout for GBit Ethernet, i.e. the pairs are 1-2, 3-6, 4-5 and 7-8.

Pin	Pair
1	D-A+
2	D-A-
3	D-B+
4	D-C+
5	D-C-
6	D-B-
7	D-D+
8	D-D-

Table 6-3 LAN Gigabit Ethernet connector pairs

### 6.3.1 Port 1

Port 1 is connected to a standard RJ-45 socket “LAN1”. It uses the SerDes Lanes 1 provided by the LS1088A CPU configured as SGMII port. The SGMII lanes connect to a Marvell PHY 88E1512P which uses a copy of the reference voltage on pin T80 of the module connector ST4 as I/O voltage (1.8V).

88E1512P		ST4		LS1088A	
Pin	Name	Pin	Signal	Pin	Name
1	S_INP	← T41	SRD-TX1+	← AD6	SD1-TX0
2	S_INN	← T42	SRD-TX1-	← AE6	SD1-TX0#
4	S_OUTP	→ T38	SRD-RX1+	→ AG6	SD1-RX0
5	S_OUTN	→ T39	SRD-RX1-	→ AH6	SD1-RX0#

Table 6-4 SerDes 1 pin assignment

### 6.3.2 Port 2

Port 2 is connected to a standard RJ-45 socket “LAN1”. It uses the SerDes Lanes 2 provided by the LS1088A CPU configured as SGMII port. The SGMII lanes connect to a Marvell PHY 88E1512P which uses a copy of the reference voltage on pin T80 of the module connector ST4 as I/O voltage (1.8V).

88E1512P		ST4		LS1088A	
Pin	Name	Pin	Signal	Pin	Name
1	S_INP	← T35	SRD-TX2+	← AD11	SD-TX3
2	S_INN	← T36	SRD-TX2-	← AE11	SD-TX3#
4	S_OUTP	→ T32	SRD-RX2+	→ AG11	SD-RX3
5	S_OUTN	→ T33	SRD-RX2-	→ AH11	SD-RX3#

Table 6-5 SerDes 2 pin assignment

### 6.3.3 Port 3

Port 3 is connected to a standard RJ-45 socket “LAN2”. It uses the SerDes Lanes 3 provided by the LS1088A CPU configured as SGMII port. The SGMII lanes connect to a Marvell PHY 88E1512P which uses a copy of the reference voltage on pin T80 of the module connector ST4 as I/O voltage (1.8V).

88E1512P		ST4		LS1088A	
Pin	Name	Pin	Signal	Pin	Name
1	S_INP	← T41	SRD-TX3+	← AD10	SD1-TX1
2	S_INN	← T42	SRD-TX3-	← AE10	SD1-TX1#
4	S_OUTP	→ T38	SRD-RX3+	→ AG10	SD1-RX1
5	S_OUTN	→ T39	SRD-RX3-	→ AH10	SD1-RX1#

Table 6-6 SerDes 3 pin assignment

### 6.3.4 Port 4

Port 4 is connected to a standard RJ-45 socket “LAN2”. It uses the Ethernet controller EC1 as RGMII port provided by the LS1088A CPU. The RGMII lanes connect to a Marvell PHY 88E1512P which uses a copy of the reference voltage on pin T80 of the module connector ST4 as I/O voltage (1.8V).

The following table shows the internal connections for Port 4.

I/O Range			88E1512P		ST4		LS1088A	
	Pull-up	Pull-down	Pin	Name	Pin	Signal	Pin	Name
1.8V			46	RX_CLK	→ T86	MII1-RXCK	→ W1	MII_RX_CLK
1.8V			43	RX_CTRL	→ T95	MII1-RXDV	→ AB1	MII_RX_DV
1.8V			44	RXD0	→ T88	MII1-RXD0	→ AA2	MII_RXD0
1.8V		4k7	45	RXD1	→ T89	MII1-RXD1	→ AA1	MII_RXD1
1.8V			47	RXD2	→ T91	MII1-RXD2	→ Y1	MII_RXD2
1.8V			48	RXD3	→ T92	MII1-RXD3	→ W2	MII_RXD3
1.8V			53	TX_CLK	← T94	MII1-TXCK	← W4	MII_TX_CLK
1.8V			50	TXD0	← T97	MII1-TXD0	← AB3	MII_TXD0
1.8V			51	TXD1	← T98	MII1-TXD1	← AA3	MII_TXD1
1.8V			54	TXD2	← T100	MII1-TXD2	← Y4	MII_TXD2
1.8V			55	TXD3	← T101	MII1-TXD3	← Y3	MII_TXD3
1.8V		4k7	56	TX_CTRL	← T103	MII1-TXEN	← AB4	MII_TXEN
1.8V	5k0		8	MDIO	↔ B87	MII1-MDIO	↔ AF2	EMI1_MDIO
1.8V	10k0		7	MDC	← B86	MII1-MDC	← AG2	EMI1_MDC
1.8V			9	CLK125	→ T83	MII1-CRS	→ AC3	EC1_GTX_CLK125

Table 6-7 Port4 pin assignment

## 6.4 PCIe Connections

The SBC-LS1088A offers three x1 lanes on the following connectors.

Serdes	ST7 (Mini-PCIe / mSATA Slot)	ST8 (Mini PCIe Slot)	ST9 (PCIe Extension Connector)	ST11 (PCIe Extension Connector)
Lane 0			✓	
Lane 4		✓		
Lane 5				✓
Lane 7	✓ (mSATA)			

Table 6-8 PCIe SerDes assignment

Basically, the carrierboard offers four x1 lanes on different connectors which may be available in combination with other MPX2 modules.

### 6.4.1 Mini-PCIe Slot

There are two mini PCIe slot on the carrierboard.

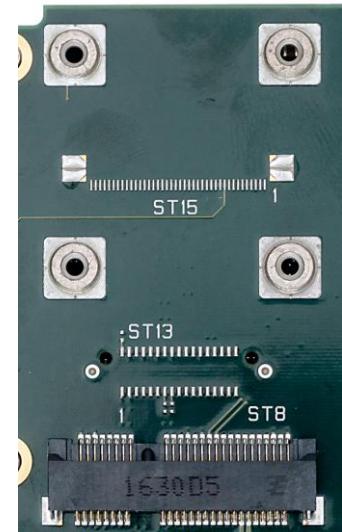
The first one can hold mPCIe cards only, mSATA is not supported.

Part Reference:	ST8
Manufacturer:	Tyco
Type:	2041119-1
Used with:	Half size mini PCIe cards are preferred



Broaching nuts for both half and full size cards are placed on the carrier board. When full size cards are used care has to be taken to choose cards that do not have parts on the bottom side accidentally shorting signals.

MicroSys recommends to use half size cards with this slot only!



Pin:			Pin:
1	WAKE#	+3.3Vaux	2
3	COEX1	GND	4
5	COEX2	+1.5V	6
7	CLKREQ#	UIM-PWR	8
9	GND	UIM-DAT	10
11	REFCLK-	UIM-CLK	12
13	REFCLK+	UIM-RST	14
15	GND	UIM-VPP	16
MECHANICAL KEY			
17	Reserved	GND	18
19	Reserved	WDIS#	20
21	GND	PERST#	22
23	PER0-	+3.3Vaux	24
25	PER0+	GND	26
27	GND	+1.5V	28
29	GND	SMB-CLK	30
31	PET0-	SMB-DAT	32
33	PET0+	GND	34
35	GND	USB-D-	36
37	GND	USB-D+	38
39	+3.3Vaux	GND	40
41	+3.3Vaux	LED_WWAN#	42
43	GND	LED_WLAN#	44
45	Reserved	LED_WPAN#	46
47	Reserved	+1.5V	48
49	Reserved	GND	50
51	Reserved	+3.3Vaux	52

Table 6-9 mPCIe Slot pinout

The following table shows the internal connections:

ST8		ST4		LS1088A	
Pin	Name	Pin	Signal	Pin	Name
33	PET4+	←	T23	SRD-TX4+	←
31	PET4-	←	T24	SRD-TX4-	←
25	PER4+	→	T20	SRD-RX4+	→
23	PER4-	→	T21	SRD-RX4-	→

Table 6-10 mPCIe Slot SerDes 4 assignment

### 6.4.2 Mini PCIe Slot / mSATA Slot

Basically, the second slot can hold both mSATA cards and mPCIe cards.

Depending on the software configuration (SerDes configuration) either mSATA or mPCIe cards can be used.

Part Reference:	ST7
Manufacturer:	Tyco
Type:	2041119-1
Used with:	Full size or half size mini PCIe or mSATA cards



Four holes for broaching nuts are designed to allow for half and full size cards to be used with this slot.

The broaching nuts for half size cards are not populated as standard to allow cards without height restrictions.

Revision 3 has NO connector JTG0 and MCU in this area!



Pin:			Pin:
1	WAKE#	+3.3Vaux	2
3	COEX1	GND	4
5	COEX2	+1.5V	6
7	CLKREQ#	UIM-PWR	8
9	GND	UIM-DAT	10
11	REFCLK-	UIM-CLK	12
13	REFCLK+	UIM-RST	14
15	GND	UIM-VPP	16
MECHANICAL KEY			
17	Reserved	GND	18
19	Reserved	WDIS#	20
21	GND	PERST#	22
23	<b>PER0+</b>	+3.3Vaux	24
25	<b>PER0-</b>	GND	26
27	GND	+1.5V	28
29	GND	SMB-CLK	30
31	PET0-	SMB-DAT	32
33	PET0+	GND	34
35	GND	USB-D-	36
37	GND	USB-D+	38
39	+3.3Vaux	GND	40
41	+3.3Vaux	LED_WWAN#	42
43	GND	LED_WLAN#	44
45	Reserved	LED_WPAN#	46
47	Reserved	+1.5V	48
49	Reserved	GND	50
51	Reserved	+3.3Vaux	52

Table 6-11 mPCIe / mSATA Slot pinout

The following table shows the internal connections:

ST7		ST4		LS1088A			
Pin	Name	Pin	Signal	Pin	Name		
33	PET0+	←	T5	SRD-TX7+	←	AD19	SD2_TX3_P
31	PET0-	←	T6	SRD-TX7-	←	AE19	SD2_TX3_N
<b>23</b>	<b>PER0-</b>	→	T2	SRD-RX7+	→	AG19	SD2_RX3_P
<b>25</b>	<b>PER0+</b>	→	T3	SRD-RX7-	→	AH19	SD2_RX3_N

Table 6-12 mPCIe Slot SerDes 7 assignment

### 6.4.3 PCIe Extension Connector 1

The PCIe Extension Connectors "ST9" and "ST11" provide basic PCIe signals. They have identical pinouts providing power, data, clock, reset and I<sup>2</sup>C signals.

Depending on the module and software configuration the data signals can also be used for other interfaces according to the SerDes configuration of the respective module.

The extension connectors interface the CRX05 carrier board with any specially developed adapter. No standard pinout is used.

Part Reference:	ST9
Manufacturer:	Würth Elektronik
Type:	687 118 140 22
Mates with:	FFC cable, 18pins, pitch 0.5mm



***The I<sup>2</sup>C port is accessible via I<sup>2</sup>C Bus 2 and the I<sup>2</sup>C multiplexer TCA9544A (address 0x70). See chapter 5.8.2 for more information.***

**NOTE**

***Devices connected to ST9 and ST11 share channel 3.***

Pin:	
1	+3.3V
2	+3.3V
3	+3.3V
4	+1.5V
5	GND
6	REFCLK-
7	REFCLK+
8	GND
9	PER0-
10	PER0+
11	GND
12	PET0-
13	PET0+
14	GND
15	I <sup>2</sup> C2D-SCL
16	I <sup>2</sup> C2D-SDA
17	GND
18	PERST#

Table 6-13 PCIe Extension connector pinout (ST9)

The following table shows the internal connections:

ST9		ST4		LS1088A	
Pin	Name	Pin	Signal	Pin	Name
13	PETO+	← T47	SRD-TX0+	← AD18	SD2-TX2
12	PETO-	← T48	SRD-TX0-	← AE18	SD2-TX2#
10	PERO+	→ T44	SRD-RX0+	→ AG18	SD2-RX2
9	PERO-	→ T45	SRD-RX0-	→ AH18	SD2-RX2#

Table 6-14 PCIe Edge Card connector SerDes 0 assignment

#### 6.4.4 PCIe Extension Connector 2

Part Reference:	ST11
Manufacturer:	Würth Elektronik
Type:	687 118 140 22
Mates with:	FFC cable, 18pins, pitch 0.5mm



*The I2C port is accessible via I2C Bus 2 and the I2C multiplexer TCA9544A (address 0x70). See chapter 5.8.2 for more information.*

**NOTE**

*Devices connected to ST9 and ST11 share channel 3.*

Pin:	
1	+3.3V
2	+3.3V
3	+3.3V
4	+1.5V
5	GND
6	REFCLK-
7	REFCLK+
8	GND
9	PER0-
10	PER0+
11	GND
12	PET0-
13	PET0+
14	GND
15	I2C2D-SCL
16	I2C2D-SDA
17	GND
18	PERST#

Table 6-15 PCIe Extension connector pinout (ST11)

The following table shows the internal connections:

ST11		ST4		LS1088A	
Pin	Name	Pin	Signal	Pin	Name
13	PET0+	← T17	SRD-TX5+	← AD16	SD2-TX1_P
12	PET0-	← T18	SRD-TX5-	← AE16	SD2-TX1_N
10	PER0+	→ T14	SRD-RX5+	→ AG16	SD2-RX1_P
9	PER0-	→ T15	SRD-RX5-	→ AH16	SD2-RX1_N

Table 6-16 PCIe Edge Card connector SerDes 5 assignment

#### 6.4.5 PCIe with external clock

To run board with external PCIe clock board has to be modified on assembly level. Please contact MicroSys if required.

## 6.5 SATA

**NOTE**

*The SATA port is not available with the SBC-LS1088A system.*

Part Reference:	ST10
Manufacturer:	3M
Type:	5607-4200-SH
Used with:	SATA cable (7pin)



The following table shows the internal connections:

ST10		ST4		LS1088A	
Pin	Name	Pin	Signal	Pin	Name
1	GND				
2	A+	← T11	SRD-TX6+	← AD19	SD2-TX3
3	A-	← T12	SRD-TX6-	← AE19	SD2-TX3#
4	GND				
5	B-	→ T9	SRD-RX6-	→ AH19	SD2-RX3#
6	B+	→ T8	SRD-RX6+	→ AG19	SD2-RX3
7	GND				

Table 6-17 SATA connector pin assignment

## 6.6 MicroSD Card Slot

The SBC-LS1088A system offers a microSD Card slot.

The microSD card can also be configured as a boot device.

Part Reference:	ST1
Manufacturer:	Yamaichi
Type:	PJS-008-2130-0
Used with:	microSD cards



The following table shows the connections of the microSD card slot:

I/O Range	ST1		ST4		LS1088A	
	Pin	Name	Pin	Signal	Pin	Name
LVTTL	1	DAT2	↔	B96	SDC-D2	↔ R1 SDHC_DAT2
LVTTL	2	CD/DAT3	↔	B95	SDC-D3	↔ T1 SDHC_DAT3
LVTTL	3	CMD	↔	B99	SDC-CMD	↔ P2 SDHC_CMD
	4	Vdd				
LVTTL	5	CLK	←	B100	SDC-CLK	← P3 SDHC_CLK
	6	Vss				
LVTTL	7	DAT0	↔	B98	SDC-D0	↔ P1 SDHC_DAT0
LVTTL	8	DAT1	↔	B97	SDC-D1	↔ R2 SDHC_DAT1
LVTTL	9	SW1	→	B90	SDC-CD#	
LVTTL	10	SW2	→	B89	SDC-WP	

Table 6-18 microSD card slot pin assignment



NOTE

**The microSD card slot uses a copy of the reference voltage on pin B81 of the module connector ST4 as I/O voltage (3.3V).**

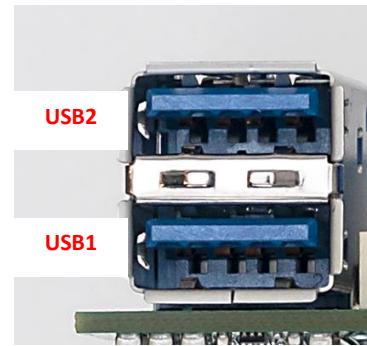
**This voltage is generated on the carrierboard.**

## 6.7 USB

The SBC-LS1088A system features a stacked USB connector for two ports.

Both USB host ports support USB super speed mode

Part Reference:	ST6
Manufacturer:	Würth Elektronik
Type:	692 141 030 100
Mates with:	USB Type A cables



### 6.7.1 USB1

The following table shows the internal connections:

ST6 (Bottom)		ST4		LS1088A			
Pin	Signal	Pin	Signal	Pin	Name		
1	Vbus+	→	B133	USB1-VBUS	→	E7	USB1_VBUS
2	D-	↔	T131	USB1-D-	↔	E6	USB1_D_M
3	D+	↔	T130	USB1-D+	↔	F6	USB1_D_P
4	GND						
5	SSRX-	→	T118	USB1-SSRX+	→	E3	USB1_RX_P
6	SSRX+	→	T119	USB1-SSRX-	→	E4	USB1_RX_M
7	GND						
8	SSTX-	←	T122	USB1-SSTX-	←	F2	USB1_TX_M
9	SSTX+	←	T121	USB1-SSTX+	←	F1	USB1_TX_P
J4							
Pin	Signal						
4	ENABLE	←	B132	USB1-EN	←	H6	USB1_DRVVBUS
3	FAULT#	→	B131	USB1-OC	→	G6	USB1_PWRFAULT
		→	B130	USB1-UID	→	F5	USB1_ID

Table 6-19 USB Host-Only Port 1 pin assignment

USB port 1 can be individually enabled and has a separate overcurrent signal.



**USB1\_PWRFAULT** is a high-active signal. A logic high level signals the port is in an overcurrent situation

### 6.7.2 USB2

The following table shows the internal connections:

ST6 (Top)		ST4		LS1088A			
Pin	Signal	Pin	Signal	Pin	Name		
1	Vbus+	→	B128	USB2-VBUS	→	C7	USB2_VBUS
2	D-	↔	T128	USB2-D-	↔	C6	USB2_D_M
3	D+	↔	T127	USB2-D+	↔	D6	USB2_D_P
4	GND						
5	SSRX-	→	T112	USB2-SSRX+	→	C3	USB2_RX_P
6	SSRX+	→	T113	USB2-SSRX-	→	C4	USB2_RX_M
7	GND						
8	SSTX-	←	T116	USB2-SSTX-	←	D2	USB2_TX_M
9	SSTX+	←	T115	USB2-SSTX+	←	D1	USB2_TX_P
J5							
Pin	Signal						
4	ENABLE	←	B127	USB2-EN	←	L4	USB2_DRVVBUS
3	FAULT#	→	B126	USB2-OC	→	M4	USB2_PWRFAULT
		→	B125	USB2-UID	→	D5	USB2_ID

Table 6-20 USB Host-Only Port 2 pin assignment

USB port 2 can be individually enabled and has a separate overcurrent signal.



**USB2\_PWRFAULT** is a high-active signal. A logic high level signals the port is in an overcurrent situation

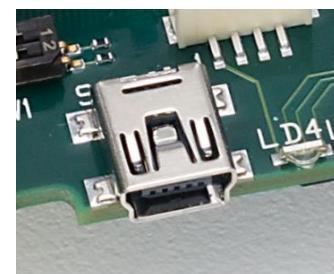
### 6.7.3 USB3

USB port 3 is not a native USB port of the CPU but converted from UART1 by means of a FT232RQ chip.

USB3 is available on an USB mini connector type B.

The port is used as the debug port of the LS1088A.

Part Reference:	ST5
Manufacturer:	Würth Elektronik
Type:	651 005 161 21
Used with:	Mini USB type B cables



The following table shows the internal connections:

ST5		ST4		LS1088A		
Pin	Signal	Pin	Signal	Pin	Name	
1	Vbus+	B37	UART1-RXD	→	H2	UART1_SIN
2	D-	J1	B38	←	H1	UART1_SOUT
3	D+		B39	→	J1	UART1_CTS#
4	ID		B40	←	J2	UART1_RTS#
5	GND					

Table 6-21 USB Host-Only Port 3 pin assignment

## 6.8 UART

The SBC-LS1088A system is provided with one serial port (UART).

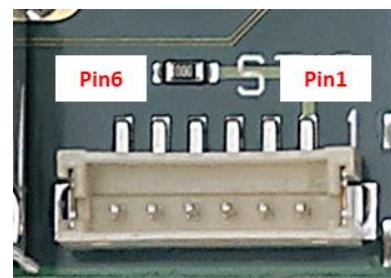
UART1 is converted to USB. See chapter 6.7.3 for details.

UART2 is available on the following extension connector including hardware handshaking with RTS/CTS. The I/O range is LVTTL.



**For RS232 or RS485 additional transceivers are necessary.  
They are not implemented on the SBC-LS1088A system.**

Part Reference:	ST12
Manufacturer:	Würth Elektronik
Type:	648 106 131 822
Mates with:	648 006 113 322



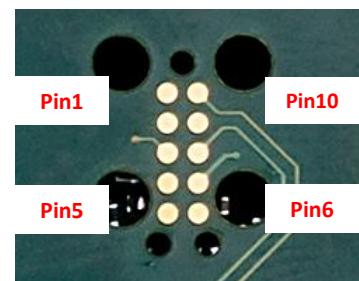
ST12		ST4		LS1088A	
Pin	Signal	Pin	Signal	Pin	Name
1	+3.3V				
2	UART2-RXD	→	B32	UART2-RXD	→
3	UART2-TXD	←	B33	UART2-TXD	←
4	UART2-RTS#	←	B35	UART2-RTS#	←
5	UART2-CTS#	→	B34	UART2-CTS#	→
6	GND				

Table 6-22 UART2 pin assignment

## 6.9 MCU Connector

The connector "MCU" is for production test R2 only. Not available on CRX05R3.

Part Reference:	MCU
Manufacturer:	Tag-Connect
Type:	TC2050-IDC-FP



MCU	
Pin	Signal
1	
2	
3	
4	
5	Please contact MicroSys
6	
7	
8	
9	
10	

Table 6-23 MCU Connector Pinout

## 6.10 JTAG Connector

### 6.10.1 JTAG on Revision R3

The JTAG signals are available on JST-BM14B-SRSS-TB connector.

Part Reference:	JTG0
Manufacturer:	JST
Type:	BM14B-SRSS-TB



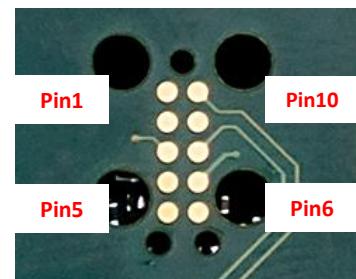
JTG0		ST4		LS1046A	
Pin	Signal	Pin	Signal	Pin	Signal
1	JTDO	←	B104	JTDO	←
2	GND			E20	TDO
3	JTDI	→	B103	JTDI	→
4	TRST#	→	B106	TRST#	→
5	+1,8V				
6	-				
7	JTCK	→	B105	JTCK	→
8	HRST#	↔	B111	HRST#	↔
9	JTMS	→	B102	JTMS	→
10	GND			G18	TMS
11	PRST#	→	B110	PRST#	→
12	GND			F9	PORESET#
13	MCU-UART-RDD	→	B114	MCU-UART-RDD	→
14	MCU-UART-TXD	←	B113	MCU-UART-TXD	←
				46	J11 MK02FN64VLH10
				49	J11 MK02FN64VLH10

Table 6-24 JTAG Connector Pinout R3

### 6.10.2 JTAG on Revision R2

The JTAG signals are available on a TAG connect footprint.

Part Reference:	JTG0
Manufacturer:	Tag-Connect
Type:	TC2050-IDC-FP



JTG0		ST4		LS1046A			
Pin	Signal	Pin	Signal	Pin	Signal		
1	JTMS	→	B102	JTMS	→	G18	TMS
2	HRST#	↔	B111	HRST#	↔	F8	HRESET#
3	+1,8V						
4	TRST#	→	B106	TRST#	→	E19	TRST#
5	JTDO	←	B104	JTDO	←	E20	TDO
6	JTCK	→	B105	JTCK	→	E18	TCK
7	GND						
8	PRST#	→	B110	PRST#	→	F9	PORESET#
9	JTDI	→	B103	JTDI	→	G17	TDI
10	-						

Table 6-25 JTAG Connector Pinout R2

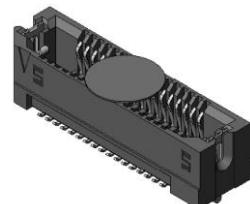
## 6.11 Aurora Connectors (optional)



**The Aurora interface is not available with the LS1088A processor.**

**NOTE**

Part Reference:	ST13
Manufacturer:	Samtec
Type:	ASP-137973-01



Pin:			Pin:
1	TX0+	VREF (1,8V)	2
3	TX0-	TCK	4
5	GND	TMS	6
7	TX1+	TDI	8
9	TX1-	TDO	10
11	GND	TRST#	12
13	TX2+	HALT#	14
15	TX2-	EVTI#	16
17	GND	EVTO#	18
19	TX3+	GEN_IO3	20
21	TX3-	RST#	22
23	GND	GND	24
25	TX4+	CLK+	26
27	TX4-	CLK-	28
29	GND	GND	30
31	TX5+	RDY#	32
33	TX5-	HRST#	34

Table 6-26 Aurora Connector Pinout

The module standard connector pinout (ST4) does not provide all signals which are necessary for the Aurora interface. Additional signals are available on the following connector "ST14". For more information please contact MicroSys.

Part Reference:	ST14
Manufacturer:	JST
Type:	SM06B-XSRS-ETB

Mates with: 06XSR-36S



Pin	Signal
1	HALT#
2	EVTI#
3	EVTO#
4	-
5	-
6	-

Table 6-27 Aurora Connector (ST14) Pinout

## 6.12 General Purpose Inputs / Outputs

The functional scope of the carrierboard has been extended by GPIOs which support a maximum of 24V at the input. The maximum output level depends on the input voltage which is limited to 24V. For lower input voltages an external voltage up to 24V can alternatively be supplied. In that case a hardware modification is necessary.

Inputs and outputs are controlled by a MAX7325ATG I<sup>2</sup>C GPIO Expander. The output pins are level shifted to either the input voltage or to the level of an externally supplied voltage. The output driver can be separately enabled and disabled. Additionally, a fault pin exists that signals a chip thermal shutdown or an overcurrent condition on any channel.

MAX7325ATG	Description
P6 (Pin7)	FAULT input: Logic low signals fault event
O14 (Pin16)	A logic high enables the GPOUT driver

GPINs:

Part Reference:	ST16
Manufacturer:	Würth Elektronik
Type:	691 382 010 006
Mates with:	691 381 000 006



Pin:	Description	MAX7325ATG
1	IN0	P0 (Pin1)
2	IN1	P1 (Pin2)
3	IN2	P2 (Pin3)
4	IN3	P3 (Pin4)
5	IN4	P4 (Pin5)
6	IN5	P5 (Pin6)

Table 6-28 GPIN connector pinout (ST16)

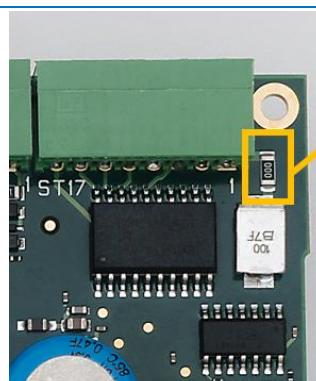
## GPOUTs:

Part Reference:	ST17
Manufacturer:	Würth Elektronik
Type:	691 382 010 008
Mates with:	691 381 000 008



Pin:	Description	MAX7325ATG
1	+VIN / +VEXT	Maximum output current on all ports together: 350mA
2	OUT6	
3	OUT5	
4	OUT4	
5	OUT3	
6	OUT2	
7	OUT1	
8	GND	

Table 6-29 GPOUT connector pinout (ST17)



Remove R154 and supply GPOUTs with external voltage on PIN1

**Pin 1 of connector ST17 is connected to the carrierboard input voltage via R154.**

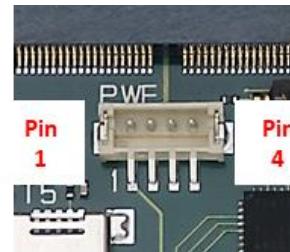
**In order to supply the GPOUT section with input voltages different from the input voltage R154 has to be removed. V\_EXT on pin1 supports input voltages from 5V to 24V.**

## 6.13 Fan Connector

The SBC-LS1088A provides a fan connector marked with „PWE“.

In case a fan is necessary MicroSys recommends using a 5V rated fan.

Part Reference:	PWE
Manufacturer:	Würth Elektronik
Type:	679 304 124 022
Mates with:	648 004 113 322



Pin:	Description
1	+5V
2	GND
3	GND
4	+VIN

Table 6-30 FAN connector pinout (PWE)

## 6.14 Smart Card Connector



**NOTE**

**THE SMART CARD INTERFACE IS NOT CONNECTED TO THE LS1088A CPU.**

**\***

Part Reference:	ST2
Manufacturer:	Würth Elektronik
Type:	693 022 010 811
Mates with:	t.b.d.



Connection von CRX05-R3:

ST2		ST4		LS1046A	
Pin	Signal Name	Pin	Description	Pin	Signal Name
1	+3,3V	-			
2	RST	←	B121 10k PU	←	C20 GPIO2_12
3	CLK	←	B122 10k PU	←	D20 GPIO2_11
4	-	-	-		
5	GND	-	-		
6	-	-	-		
7	I/O	↔	B123 10k PU	↔	A19 GPIO2_10
8	-	-	-		

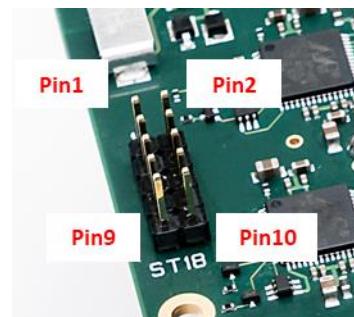
Table 6-31 Smart Card connector pinout (ST2)

## 6.15 emBRICK Connector

**NOTE**

**THE emBRICK INTERFACE IS CURRENTLY NOT SUPPORTED**

Part Reference:	ST18
Manufacturer:	Würth Elektronik
Type:	613 005 211 21
Mates with:	Standard 2.54mm dual row socket



Pin	Signal Name	Connection
1	SEL_OUT	MAX7325ATG O15 (Pin17)
2	MOSI#	SC18IS602BIPW MOSI (Pin6)
3	MISO#	SC18IS602BIPW MISO (Pin5)
4	CLK#	SC18IS602BIPW SPICLK (Pin11)
5	+3,3V	
6	GND	
7	GND	
8	GND	
9	+VIN	
10	+VIN	

Table 6-32 emBRICK connector pinout (ST18)

# 7 Switches, Buttons and Jumpers

## 7.1 Boot Device Switch

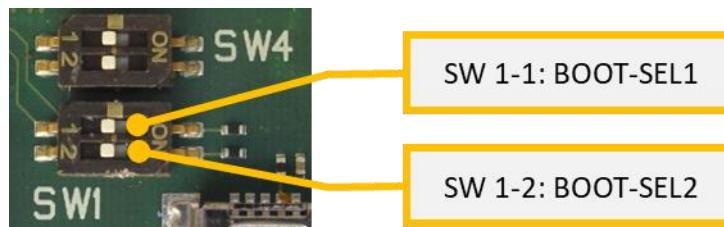


Figure 7-1 Boot Device Switch

The boot device can be selected by the switch “SW1”.

The boot device switches implement a maximum of four possible boot devices. The following boot devices are supported by the LS1088A:

Setting	SW 1-1	SW 1-2	Boot device	Features	Boot location
	OFF	OFF	SPI Flash		module
	OFF	ON	NAND Flash		module
	ON	OFF	SD/MMC	SD/MMC Bus width: 8 bit SPI-CS0# [PIN-B70] is <u>NOT</u> accessible	carrier board
	ON	ON	SD/MMC	SD/MMC Bus width: 4 bit SPI-CS0# [PIN-B70] is <u>NOT</u> accessible	carrier board

Table 7-1 Boot device settings



**SW1 inverts the logic levels of the BOOT-SELx pins. By setting the switch to ON the corresponding pin is actually pulled low (grounded).**

The following table shows the internal connections of the BOOT-SEL pins:

SW1		ST4		Microcontroller			
Switch	Signal	Pin	Signal	Pin	Name		
1-1	BOOT-SEL1	→	T134	BOOT-SEL1	→	61	PTD4
1-2	BOOT-SEL2	→	T133	BOOT-SEL2	→	62	PTD5

Table 7-2 BOOT-SELx pin assignment

## 7.2 Board Configuration Switch

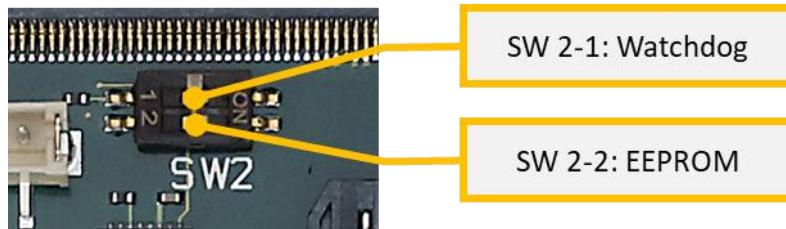


Figure 7-2 Board Configuration Switch

The board configuration switch influences the behavior of the watchdog and the I<sup>2</sup>C address of the EEPROM on I<sup>2</sup>C Bus1:

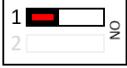
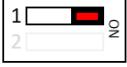
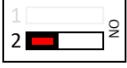
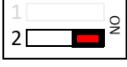
Setting	SW 2-1	SW 2-2	Description
	OFF	-	Watchdog disabled
	ON	-	Watchdog active
	-	OFF	EEPROM J25: address 0x57
	-	ON	EEPROM J25: address 0x55

Table 7-3 Configuration switch settings

## 7.3 PCIe selection: root complex / endpoint

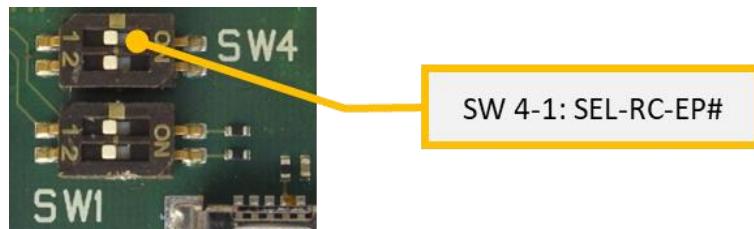


Figure 7-3 PCIe selection Switch

The PCIe configuration switch influences the behavior of root complex or endpoint.

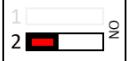
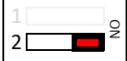
Setting	SW 4-1	SW 4-2	Description
	OFF	-	PCIe = root complex
	ON	-	PCIe = endpoint
	-	OFF	Not used
	-	ON	Not used

Table 7-4 PCIe Configuration switch settings

## 7.4 Reset Button

Pressing the reset switch “SW3” triggers a Hard Reset.

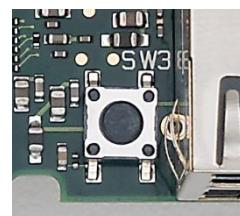


Figure 7-3 Reset Button

SW3 is connected to the reset input of a MAX6751KA29 chip via additional logic. The resulting open drain reset signal is then inverted and fed to the microcontroller.

The following table shows the internal connections:

SW3		J17		ST4		Microcontroller	
Pin	Signal	Pin		Pin	Signal	Pin	Name
1 & 3	+3,3V						
2 & 4	RST-BTN (\$39166)	→	1	7	→ T136	RST-IN#	→ 52 PTC7

Table 7-4 Reset button pinout

# 8 LEDs

## 8.1 RJ45 LEDs

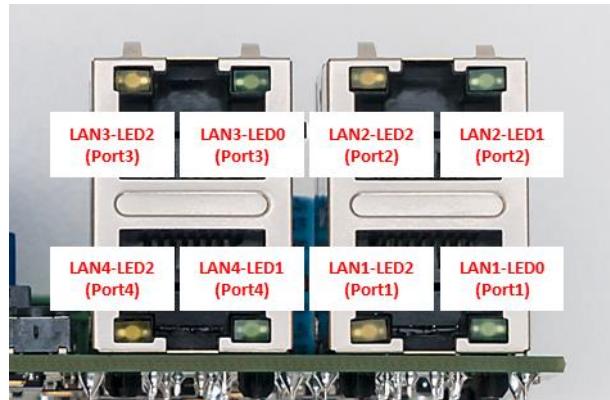


Figure 8-1 RJ 45 LEDs

The following table summarizes the RJ45 LEDs of the SBC-LS1088A:

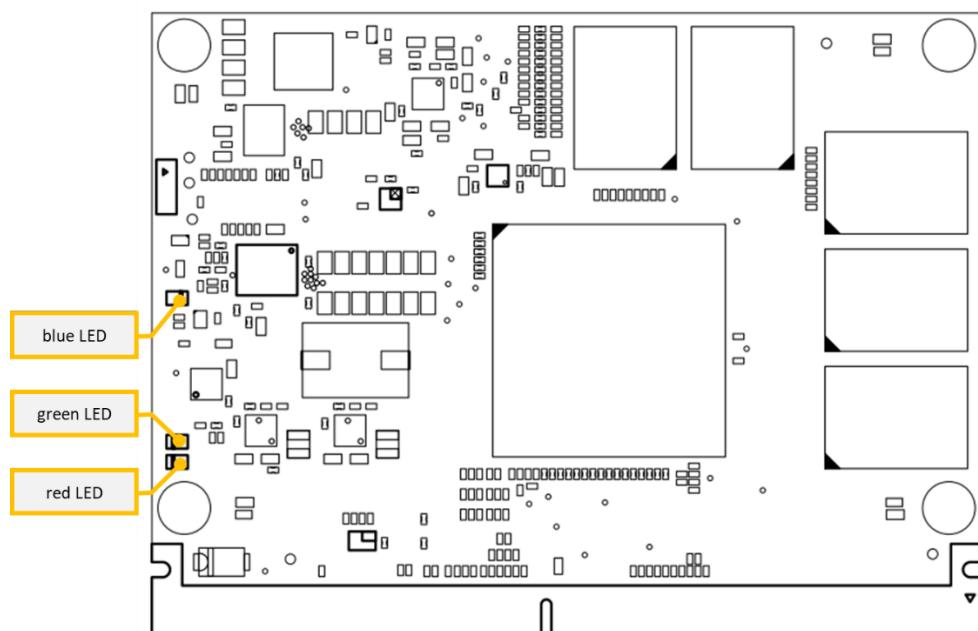
Part Reference	Source	Signal Name	Function
LAN1-A	J8	LAN1-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN1-A	J8	LAN1-LED2	Yellow LED: off
LAN1-B	J10	LAN2-LED1	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN1-B	J10	LAN2-LED2	Yellow LED: off
LAN2-B	J12	LAN3-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN2-B	J12	LAN3-LED2	Yellow LED: off
LAN2-A	J14	LAN4-LED1	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN2-A	J14	LAN4-LED2	Yellow LED: off

Table 8-1 Indicator LEDs

## 8.2 Power And Reset LEDs

Part Reference	Source	Signal Name	Function
LD1	ST3	VEXT	Power (VEXT) On
LD2	ST4	CB-RST#	Carrier board reset active
LD3	J17 / SW3	RST-IN#	<ul style="list-style-type: none"> <li>Power on the carrier is not ok</li> <li>watchdog reset is active</li> <li>manual reset is triggered</li> </ul>

Table 8-2 Indicator LEDs - Carrier board



Colour	Function
Green	LED ON: Power-up sequence of the module is finished, power is good LED OFF: Power fail
Red	LED ON: Module reset is active LED OFF: Reset is inactive
Blue	General Purpose LED

Table 8-3 Indicator LEDs – Module

## 8.3 RGB LEDs

The SBC-LS1088A provides a RGB LED driver controlling four RGB LEDs.



**I<sup>2</sup>C address 0x68 is existing twice on I<sup>2</sup>C-1 bus.**

**Therefore, the so-called “All Call I<sup>2</sup>C address” of the TLC59116IRHBR RGB LED driver has to be disabled before GP input pins of the MAX7325 port expander can be read correctly. This can be achieved by setting the default value 1 of Bit 0 in MODE1 register to 0.**

The following table shows how the LEDs are mapped to the driver outputs:

Part Reference	LED Driver Output	LED Output Register
LD4	LED0	0x14
	LED1	
	LED2	
	LED3 is not connected	
LD7	LED4	0x15
	LED5	
	LED6	
	LED7 is not connected	
LD6	LED8	0x16
	LED9	
	LED10	
	LED11 is not connected	
LD5	LED12	0x17
	LED13	
	LED14	
	LED15 is not connected	

Table 8-4 Indicator LEDs – Mapping

## 9 Software

### 9.1 U-Boot

The SBC-LS1088A uses a U-Boot as standard boot loader, which is integrated in the board's QSPI Flash memory on delivery. NAND boot is not any longer recommended due to reliability and thus not included in standard delivery.

Additionally, there's a U-Boot version available to be placed on microSD card, if both other boot options should fail for some reason.

Either boot option can be selected by the Boot Device Switch (see chapter 7).

### 9.2 Operating System Support

MicroSys Electronics GmbH offers Linux and Microware OS-9 RTOS support for the board.

Other Operating Systems are available on request only.

If you should have ordered a Starter Kit, the most recent Linux will already be installed in the board's flash, so you can start to develop and test your application right away.

# 10 Appendix

## 10.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

CPU.....	<i>Central Processing Unit</i>
DC .....	<i>Direct Current</i>
DDR4.....	<i>Double Data Rate Memory fourth-generation</i>
EC .....	<i>Ethernet Controller</i>
ESD.....	<i>Electrostatic Discharge</i>
Gbps.....	<i>Gigabit per second, Gigabit per second</i>
GND .....	<i>Ground</i>
GPL .....	<i>General Public License</i>
I2C.....	<i>Inter-Integrated Circuit</i>
JTAG .....	<i>Joint Test Action Group</i>
LAN .....	<i>Local Area Network</i>
LED .....	<i>Light Emitting Diode</i>
LVTTL.....	<i>Low Voltage Transistor–Transistor Logic</i>
MCU .....	<i>Microcontroller Unit</i>
MMC.....	<i>Multimedia Card</i>
mPCIe .....	<i>Mini Peripheral Component Interconnect Express</i>
mSATA.....	<i>Mini Serial Advanced Technology Attachment</i>
RGMII.....	<i>Reduced Gigabit Media-independent Interface</i>
RTC.....	<i>Real Time Clock</i>
SBC.....	<i>Single Board Computer</i>
SD .....	<i>Secure Digital</i>
SDIO.....	<i>Secure Digital Input Output</i>
SDRAM .....	<i>Synchronous Dynamic Random Access Memory</i>
SerDes .....	<i>Serializer/Deserializer</i>
SOM .....	<i>System On Module</i>
UART.....	<i>Universal Asynchronous Receiver Transmitter</i>
USB.....	<i>Universal Serial Bus</i>

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# 11 History

Date	Version	Change Description
2017-10-09	<b>2.0</b>	Release Version for carrier CRX05 Revision 2
2017-11-09	<b>2.1</b>	Added I2C1 address 0x00 in Table 5-7
2018-07-16	<b>2.2</b>	Table 2-2: add LED colors Operating voltage change to 9V – 30V PCIe portcount correction
2019-01-28	<b>2.3</b>	Added differences CRX05 carrier revision 2 to revision 3 (2.4.1)
2019-04-26	<b>2.4</b>	Removed typos Removed I2C-2 and added I2C-4 in chapter 5.8
2024-03-07	<b>2.5</b>	NAND Boot not any longer recommended 9.1 Removed memory layout due to frequent changes in BSP Minor spelling corrections

Table 11-1 Document history